CLAIMS

The following listing of claims replaces all prior versions and listings of claims in the above-referenced application:

1. (Currently amended) A system comprising:

shared system registers, each shared system register including ~~one or more~~ bits defining an access protocol, and one or more bits representing data; and

N processors, N≥ 2, where N is an integer, each of the N processors accessing the shared system registers, wherein said ~~one or more~~ bits defining the access protocol include ~~one or more~~ bits that define a register access type comprising access modes for each of the N processors.

2. (Canceled)

3. (Previously presented) A system, as defined in claim 1, the register access type being selected from a group that includes READ, READ/CLEAR, READ/SET, and READ/WRITE.

4. (Previously presented) A system, as defined in claim 3, further comprising at least one programmable configuration register operative to encode and store said one or more bits defining the access protocol, each of said at least one programmable configuration register corresponding to one of the shared system registers.

5. (Previously presented) A system, as defined in claim 4, wherein:

each programmable configuration register consists of N*2 bits; and

the configurable register access types are encoded into 2 bits.

6. (Currently amended) A system, as defined in claim [~~3~~] 1, the access protocol encoded and provided as input signals to a hardware design.

7. (Currently amended) A system, as defined in claim [3] 1, the access protocol encoded and selected as a build-time option in a hardware design source code.

8. (Currently amended) A system, as defined in claim [3] 1, the access protocol further including an arbitration priority.

9. (Previously presented) A system, as defined in claim 8, comprising programmable configuration registers operative to encode and store the access protocol, each programmable configuration register corresponding to one of the shared system registers.

10. (Previously presented) A system, as defined in claim 9, wherein:
N is 2; and
each programmable configuration register includes 5-bits, 2 bits represent the access type of one of the two processors, 2 bits represent the access type of the other of the two processors, and 1 bit represents the arbitration priority.

11. (Previously presented) A system, as defined in claim 9, wherein:
each programmable configuration register consists of N*(2+ceiling($\log_2$N)) bits; and
the access protocol including the four access types are encoded into 2 bits per processor and the arbitration priority encoded into ceiling($\log_2$N) bits.

12. (Previously presented) A system, as defined in claim 8, the access protocol encoded and selected as a build-time option in a hardware design source code.

13. (Previously presented) A system, as defined in claim 8, the access protocol encoded and provided as input signals to a hardware design.